

## ELECTRONIC INFORMATION DISCLOSURE STATEMENT

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PATENT

MANUFACTURER

PERFORMANCE

METHOD AND STRUCTURE FOR DOUBLE SPACER CMOS WITH OPTIMIZED NFET/PFET

## Title of Invention

METHOD AND STRUCTURE FOR DOUBLE SPACER CMOS WITH OPTIMIZED NFET/PFET

Application Number:

Confirmation Number:

First Named Applicant: Sadanand Deshpande

Attorney Docket Number: FIS920030397US1

Search string: ( 5663586 or 5641698 or 5747373 or 5824588 or 6207519 or 6306702 or 6500765 or 6503806 or 6617229 or 5465342 or 20020142556 ).pn.

## US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

Init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	5663586	1997-09-02	Lin			
	2	5641698	1997-06-24	Lin			
	3	5747373	1998-05-05	Yu			
	4	5824588	1998-10-20	Liu			
	5	6207519	2001-03-27	Kim et al			
	6	6306702	2001-10-23	Hao et al			
	7	6500765	2002-12-31	Kao et al			
	8	6503806	2003-01-07	Kim			
	9	6617229	2003-09-09	Kim			
	10	5465342	1995-11-07	Walsh			

## US Published Applications

Note: Applicant is not required to submit a paper copy of cited US Published Applications

Init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
	1	20020142556	2002-10-03	Kim			

## Signature

Examiner Name

Date